REMARKS

Section A of these Remarks summarizes the status of the pending claims. The remaining sections respond to the rejections and objections of the Office Action in the order in which they appeared in the Action.

A. Status of Claims:

Claims 1-56 are pending in the application. Claims 45-56 are withdrawn from consideration. Claims 1-3, 6, 8-26, and 35-44 were rejected under 35 USC 102(b) as being anticipated by Feth et al., US Patent No. 4,338,622. Claims 4 and 5 were rejected under 35 USC 103(a) as being unpatentable over Feth et al. in view of Harari, US Patent No. 4,417,325. Claim 7 was rejected under 35 USC 103(a) as being unpatentable over Feth et al.

Claims 27-34 were objected to.

B. 102(b) Rejections: Claims 1-3, 6, 8-26, and 35-44

Claims 1-3, 6, 8-26, and 35-44 were rejected under 35 USC 102(b) as being anticipated Feth et al.

As amended, claim 1 recites a semiconductor device comprising: a silicide layer; and a grown dielectric antifuse layer on and in contact with the silicide layer, wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device.

An antifuse is an element in an integrated circuit having a function opposite that of a fuse: An antifuse, when first created, electrically separates two conductive elements. Once a sufficiently high voltage is applied across the antifuse, dielectric breakdown occurs, and the antifuse is permanently altered, rendering it conductive.

The grown dielectric layer 238 of Feth et al. is a dielectric layer adapted to permanently provide electrical isolation between conductive elements. It is not a dielectric antifuse layer, which is intended, during normal operation of the device, to suffer dielectric breakdown, forming a permanent electrical connection between conductive elements that were previously isolated.

Thus as amended, claim 1 and its dependent claims distinguish over Feth et al.

Additionally, in rejecting claims 10 and 11, the Examiner asserts:

> ... Feth discloses the device of claim 9, wherein the conductive layer forms a portion of a Schottky diode.

The Examiner does not identify disclosure in Feth et al. that layer 252 is a portion of a Schottky diode. The only mention of a Schottky diode is in reference to "the N type collector region doping levels," at col. 13, lines 51-59. This is described in relation to the embodiments of Figs. 6a-6l and 7a-7l, not to the embodiment of Figs. 8a-8l identified by the Examiner. Further, the collector regions of the embodiment of Figs. 8a-8l are regions 240 and 242 (col. 12, lines 10-13), not layer 252. There is no teaching in Feth et al. that layer 252 is a portion of a Schottky diode. The Examiner uses the same rationale in the rejections of claims 16, 17, 36, and 41.

In rejecting claim 14, the Examiner finds a monolithic three dimensional memory array in the device of Feth et al. A monolithic three dimensional memory array, however is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, US Patent No. 5,915,167, "Three dimensional structure memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

Fabrication of a stacked memory array formed above a substrate is described in the instant application (see paragraphs [0068] and [0079], for example), as well as in Petti et al. (incorporated by reference in paragraph [0002] of the instant application) in and Herner et al., US Patent Application No. 10/326470 (incorporated by reference in paragraph [0080] of the instant application.)

All of the storage cells of Feth et al. are formed having a portion of the cell *in* the wafer substrate (layers 206 and 208 of Figs. 8a-8l, for example; also see col. 5, lines 33-36), and thus only one memory level is formed. In a monolithic three dimensional memory array, multiple memory levels are formed stacked above a single substrate. The same rationale applies to the rejections of claims 20, 26, 39, and 44.

Applicants have shown that Feth et al. do not teach a grown dielectric antifuse layer, nor a Schottky diode, nor a monolithic three dimensional memory array, and respectfully request reconsideration.

C. 103(a) Rejection, Claims 4 and 5

Claims 4 and 5 were rejected under 35 USC 103(a) as being unpatentable over Feth et al. in view of Harari.

Claim 4 has been amended to recite a semiconductor device comprising: a silicide layer; and a grown dielectric antifuse layer on and in contact with the silicide layer, wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device, wherein the silicide is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, palladium silicide, tantalum silicide, and niobium silicide, wherein the grown dielectric antifuse layer comprises nitrogen. (This summary includes the limitations of claim 4 and of claims 1 and 2, from which it depends.)

Claim 5 adds the limitation that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride.

The Examiner finds a silicon nitride layer used in Harari et al. and argues that:

> It would have been obvious to one skilled in the art at the time of the invention to use a silicon nitride layer as disclosed by Harari et al. in place of the silicon oxide layer of Feth for the purpose, for example, of maintaining good isolation between conductive layers.

Claims 4 and 5 depend from amended claim 1, and thus distinguish over Feth et al. for the reasons described in Section B of this response.

In addition, however, Applicant points out that the claim calls for a grown dielectric antifuse layer comprising nitrogen, or comprising silicon nitride or oxynitride, which is grown on a silicide layer. Feth et al. apparently show a *silicon dioxide* layer 238 grown on a silicide layer 230. It is not conventional to thermally grow a *nitride* or oxynitride layer on a silicide layer, however, as recited in the claim.

The dielectric layer of Harari et al. referred to by the Examiner is layer 110 which may be "thermal silicon dioxide or thermal silicon nitride ..." (col. 4, line 33). Applicant points out that if layer 110 is thermal silicon nitride, it is grown on gate 103, which is polysilicon (col. 4, line 4), not silicide or capped with silicide. Feth et al. teach an oxide layer grown on a silicide (though not an antifuse layer), while Harari et al. teach a *nitride* layer grown on *polysilicon*. Neither of the references, however, teaches or suggests growing a nitride or oxynitride layer on a silicide, as in the claim.

Applicant has shown that the proposed combination of references fails to teach or suggest each and every element of the claim, and respectfully requests reconsideration of the 35 USC 103(a) rejection of claims 4 and 5.

D. 103(a) Rejection, Claim 7

Claim 7 was rejected under 35 USC 103(a) as being unpatentable over Feth et al.

Claim 7 depends from amended claim 1, and thus distinguishes over Feth et al. for the reasons described in Section B of this response.

In addition, as amended, claim 7 recites a semiconductor device comprising: a silicide layer; and a grown dielectric antifuse layer on and in contact with the silicide layer, wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device, wherein the silicide is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, palladium silicide, tantalum silicide, and niobium silicide, further comprising; a conductive layer on and in contact with the grown dielectric antifuse layer, wherein the grown dielectric antifuse layer is less than about 50 angstroms thick. (This summary includes the limitations of claim 7 as well as those of claims 1, 2, and 6, from which it depends.)

The Examiner asserts:

> ... it would have been obvious to one skilled in the art at the time the invention was made to make the grown dielectric antifuse layer about or less than 50 angstroms thick, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Applicant points out, however, that the general conditions of the claim have not been disclosed in Feth et al. As amended, claim 7 recites a grown dielectric antifuse layer; layer 238 of Feth et al. is not a dielectric antifuse layer, and instead is providing permanent electric isolation between conductive elements. The roles of these dielectric layers are different, and thus the criteria used to determine preferred thickness of these layers is unrelated.

Applicant respectfully requests reconsideration.

E. Claim Objections

Claims 27-34 were objected to as being dependent upon a rejected base claim, but were considered allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants appreciate the indication of allowable subject matter.

CONCLUSION

In view of these amendments and remarks, Applicant submits that this application is in condition for allowance. Reconsideration is respectfully requested. **To expedite prosecution, Applicant respectfully requests an interview to discuss the references.** If the Examiner has any questions, he is encouraged to contact the undersigned agent at (408) 869-2921.

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Date

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